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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,284	SAKAMA ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *41-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The examiner has considered the items listed on the Information Disclosure Statement filed 09/24/2003 to the extent possible: the full text of the specification, as opposed to the English abstracts, of items JP 7-335900, JP 8-078329, JP 10-135468 and JP 10-135469, are in the Japanese language. Furthermore, the examiner has not considered item by Terada et al, "Half-V Switching Mode FLCD" (item 1), because this item in the information disclosure statement filed 09/24/03 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered. A signed copy of Form PTO-1449 is herewith included with this office action, with the above exception noted thereon for said item by Terada et al.

Claim Objections

1. ***Claims 41, 45, 48, 51 and 54*** objected to because of the following informalities: the wording "first semiconductor film" (line 14 in claim 41, line 10 in claim 45, line 10 in claim 51, line 10 in claim 54) should be replaced by: "first semiconductor layer". Appropriate correction is required.

2. ***Claims 41, 45, 48, 51 and 54*** objected to because of the following informalities: the wording "second and third semiconductor films" (line 15 in claim 41, line 11 in claim

45, line 11 in claim 51, line 11 in claim 54) should be replaced by: "first semiconductor layer". Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 41, 44, 45, 48, 51, 54 and 57-61*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki et al (5,804,878) in view of Yamazaki et al (JP408055847A) (as made of record in IDS), for which Yamazaki et al (5,970,384) (also made of record in IDS), - of which JP408055847A is Foreign Priority, serves as translation.

Miyazaki et al teach a semiconductor device comprising a pixel portion and a driver circuit on a substrate (cf. col. 10, l. 52-col. 11, l. 3; Figures 1 and 6), comprising: a base film 2 (corresponding to element with numeral 2 in Figure 1, and visible in Figure 6);

first, second and third semiconductor layers over said base film (said semiconductor layers corresponding to element with numeral 5 in Figure 1 (col. 7, l. 16-19) and corresponding to the semiconductor layers underneath each of three thin film transistors (pixel transistor TFT3 and driver transistors TFT1, TFT2, respectively, in Figure 6);

a first gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent to said first semiconductor layer with a gate insulating film 6 (cf. col. 7, l. 16-18) interposed therebetween, wherein a first LDD region (corresponding to region 209 or 210 in Figure 2; col. 9, l. 30-38) in said first semiconductor layer (of TFT3) is not overlapped with said first gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that film 507 (207) is used as mask; col. 9, l. 30-38);

a second gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent said second semiconductor layer with said gate insulation film 6 (cf. col. 11, l. 13-18) therebetween, a second LDD region in said semiconductor layer (of TFT2) is overlapped with said second gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that the anode oxide film 506 is used as mask; col. 9, l. 30-38);

a third gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent said third semiconductor layer with said gate insulation film 6 (cf. col. 11, l. 13-18) therebetween, a third LDD region in said semiconductor layer (of TFT3) is overlapped with said third gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that the anode oxide film 505 is used as mask; col. 9, l. 30-38); and

wherein said pixel portion comprises said first semiconductor "film" (actually: layer: see under "Objections to Claims"), and said driver portion comprises said second and third semiconductor "films" (actually: layers: see under "Objections to Claims") (cf. col. 10, l. 52-61).

Miyazaki et al do not necessarily teach the limitation defined in the final three lines of claim 41.

However, it would have been obvious to include said limitation in view of *Yamazaki et al*, who, in a patent on an improved composition of gate insulation films in thin film transistors, - hence closely related art, teach the selection of hydrogenated silicon oxynitride of which the hydrogenation is reduced (cf. abstract): starting from a silicon dioxide film (concentration thus being 2/3 = 66.7 % oxygen, thus falling well within the claimed range of 55 to 70 percent) wherein through annealing by NH_3 nitrogen bonds are created so as to reduce the number of un-paired bonds (col. 4, l. 1-60) and in particular replacing the deleterious Si-H bonds and Si-OH bonds through replacement of the a substantial portion of the hydrogen with nitrogen (cf. col. 7, l. 1-32), with a stated nitrogen concentration of typically between 0.1 and 6 atomic % of N (col. 11, l. 49-54), thus substantially overlapping the claim limitation of 0.1 to 6 atomic % of N. Because the nitrogen only is able to replace pre-existing hydrogen and the hydrogen is further reduced through an annealing step (cf. abstract) it can be concluded logically that the H concentration is substantially less than 6 atomic %. Furthermore, the single Si-H and Si-OH bonds are substantially due to water penetration (cf., e.g., col. 2, l. 61 – col. 3, l. 3) and hence occur in substantially equal abundance, which as both H are replaced by nitrogen bonds (cf. col. 7, l. 18-23) implies a reduction by substantially half the amount of N introduced, i.e., substantially less than 6/2 = 3 atomic % H. Applicant does not explain in the Specification why the difference between the H concentration ranger of between 0 and 3 atomic % as inferred from Yamazaki et al and the range claimed (between 0.1 and 3 atomic %) is critical to the invention. Applicant is reminded that it has been held that a *prima facie* case of obviousness typically exists when the

ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). *Motivation* to include the teaching by Yamazaki et al in the invention by Miyazaki et al at least derives from the resulting improvement of the gate insulation film's insulating properties through the removing of single hydrogen bonds.

On claim 44: said substrate is a glass substrate (cf. col. 8, l. 27-35).

On claims 45 and 51 (which is a substantial duplicate of claim 45, see "Double Patenting"): Miyazaki et al teach a semiconductor device comprising a pixel portion and a driver circuit on a substrate (corresponding with element 201 in Figure 1) (cf. col. 8, l. 28-36, 10, l. 52-col. 11, l. 3; Figures 1 and 6), comprising:

first, second and third semiconductor layers over said substrate (said semiconductor layers corresponding to element with numeral 5 in Figure 1 (col. 7, l. 16-19) and corresponding to the semiconductor layers underneath each of three thin film transistors (pixel transistor TFT3 and driver transistors TFT1, TFT2, respectively, in Figure 6);

a first gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent to said first semiconductor layer with a gate insulating film 6 (cf. col. 7, l. 16-18) interposed therebetween, wherein a first LDD region (corresponding to region 209 or 210 in Figure 2; col. 9, l. 30-38) in said first semiconductor layer (of TFT3) is not

overlapped with said first gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that film 507 (207) is used as mask; col. 9, l. 30-38);

a second gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent said second semiconductor layer with said gate insulation film 6 (cf. col. 11, l. 13-18) therebetween, a second LDD region in said semiconductor layer (of TFT2) is overlapped with said second gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that the anode oxide film 506 is used as mask; col. 9, l. 30-38);

wherein said pixel portion comprises said first semiconductor "film" (actually: layer: see under "Objections to Claims"), and said driver portion comprises said second and third semiconductor "films" (actually: layers: see under "Objections to Claims") (cf. col. 10, l. 52-61).

Miyazaki et al do not necessarily teach the limitation defined in the final three lines of claim 45.

However, it would have been obvious to include said limitation in view of *Yamazaki et al*, who, in a patent on an improved composition of gate insulation films in thin film transistors, - hence closely related art, teach the selection of hydrogenated silicon oxynitride of which the hydrogenation is reduced (cf. abstract): starting from a silicon dioxide film (concentration thus being 2/3 = 66.7 % oxygen, thus falling well within the claimed range of 55 to 70 percent) wherein through annealing by NH_3 nitrogen bonds are created so as to reduce the number of un-paired bonds (col. 4, l. 1-60) and in particular replacing the deleterious Si-H bonds and Si-OH bonds through replacement of the a substantial portion of the hydrogen with nitrogen (cf. col. 7, l. 1-32),

with a stated nitrogen concentration of typically between 0.1 and 6 atomic % of N (col. 11, l. 49-54), thus substantially overlapping the claim limitation of 0.1 to 6 atomic % of N. Because the nitrogen only is able to replace pre-existing hydrogen and the hydrogen is further reduced through an annealing step (cf. abstract) it can be concluded logically that the H concentration is substantially less than 6 atomic %. Furthermore, the single Si-H and Si-OH bonds are substantially due to water penetration (cf., e.g., col. 2, l. 61 – col. 3, l. 3) and hence occur in substantially equal abundance, which as both H are replaced by nitrogen bonds (cf. col. 7, l. 18-23) implies a reduction by substantially half the amount of N introduced, i.e., substantially less than 6/2 = 3 atomic % H. Applicant does not explain in the Specification why the difference between the H concentration ranger of between 0 and 3 atomic % as inferred from Yamazaki et al and the range claimed (between 0.1 and 3 atomic %) is critical to the invention. Applicant is reminded that it has been held that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). *Motivation* to include the teaching by Yamazaki et al in the invention by Miyazaki et al at least derives from the resulting improvement of the gate insulation film's insulating properties through the removing of single hydrogen bonds.

On claims 48 and 54 (claim 54 is a substantial duplicate of claim 48, see "Double Patenting"): Miyazaki et al teach a semiconductor device comprising a pixel portion and

a driver circuit on a substrate (corresponding with element 201 in Figure 1) (cf. col. 8, l. 28-36, 10, l. 52-col. 11, l. 3; Figures 1 and 6), comprising:

first, second and third semiconductor layers over said substrate (said semiconductor layers corresponding to element with numeral 5 in Figure 1 (col. 7, l. 16-19) and corresponding to the semiconductor layers underneath each of three thin film transistors (pixel transistor TFT3 and driver transistors TFT1, TFT2, respectively, in Figure 6);

a first gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent to said first semiconductor layer with a gate insulating film 6 (cf. col. 7, l. 16-18) interposed therebetween, wherein a first LDD region (corresponding to region 209 or 210 in Figure 2; col. 9, l. 30-38) in said first semiconductor layer (of TFT3) is not overlapped with said first gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that film 507 (207) is used as mask; col. 9, l. 30-38);

a second gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent said second semiconductor layer with said gate insulation film 6 (cf. col. 11, l. 13-18) therebetween, a second LDD region in said semiconductor layer (of TFT2) is overlapped with said second gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that the anode oxide film 506 is used as mask; col. 9, l. 30-38);

wherein said pixel portion comprises said first semiconductor "film" (actually: layer: see under "Objections to Claims"), and said driver portion comprises said second and third semiconductor "films" (actually: layers: see under "Objections to Claims") (cf. col. 10, l. 52-61).

Miyazaki et al do not necessarily teach the limitations on composition of the gate insulation film and on thickness of said gate insulation film as defined in the final five lines of claim 48, except that Miyazaki et al do teach the gate insulation film to have a thickness between 70 and 150 nm (col. 8, l. 43-45), which range overlaps with the range as claimed in the final two lines of claim 48. Furthermore, while following the teaching by Yamazaki et al the gate insulation film by Miyazaki et al is replaced by a hydrogenated oxynitride film as explained above, the thickness of said hydrogenated oxynitride film is 100 nm (col. 12, l. 64-67), which also falls in the range as claimed. Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as claimed do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

Furthermore, it would have been obvious to include the limitation on composition of said gate insulation film in view of *Yamazaki et al*, who, in a patent on an improved composition of gate insulation films in thin film transistors, - hence closely related art, teach the selection of hydrogenated silicon oxynitride of which the hydrogenation is reduced (cf. abstract): starting from a silicon dioxide film (concentration thus being 2/3 = 66.7 % oxygen, thus falling well within the claimed range of 55 to 70 percent) wherein through annealing by NH_3 nitrogen bonds are created so as to reduce the number of un-paired bonds (col. 4, l. 1-60) and in particular replacing the deleterious Si-H bonds and Si-OH bonds through replacement of the a substantial portion of the hydrogen with

nitrogen (cf. col. 7, l. 1-32), with a stated nitrogen concentration of typically between 0.1 and 6 atomic % of N (col. 11, l. 49-54), thus substantially overlapping the claim limitation of 0.1 to 6 atomic % of N. Because the nitrogen only is able to replace pre-existing hydrogen and the hydrogen is further reduced through an annealing step (cf. abstract) it can be concluded logically that the H concentration is substantially less than 6 atomic %. Furthermore, the single Si-H and Si-OH bonds are substantially due to water penetration (cf., e.g., col. 2, l. 61 – col. 3, l. 3) and hence occur in substantially equal abundance, which as both H are replaced by nitrogen bonds (cf. col. 7, l. 18-23) implies a reduction by substantially half the amount of N introduced, i.e., substantially less than 6/2 = 3 atomic % H. Applicant does not explain in the Specification why the difference between the H concentration ranger of between 0 and 3 atomic % as inferred from Yamazaki et al and the range claimed (between 0.1 and 3 atomic %) is critical to the invention. Applicant is reminded that it has been held that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). *Motivation* to include the teaching by Yamazaki et al in the invention by Miyazaki et al at least derives from the resulting improvement of the gate insulation film's insulating properties through the removing of single hydrogen bonds.

On claims 57, 58, 59, 60, 61: said second semiconductor layer comprises a second source region and a second drain region (doped regions 208 and 211, see

Figures 1, 6 and 7) (col. 7, 30-38, and elements 8; cf. col. 11, l. 13-18), and a second channel region between said second source and second drain regions (see claim 23 in Miyazaki et al; furthermore, a channel between source and drain is utterly inherent to any field effect transistor), said second LDD region is between said second channel and drain regions (element 209 is in between the channel, as the remaining portion after source/drain implementation of semiconductor region 203, and source/drain regions 208/211; cf. Figure 1), and said second source region is in (electrical) contact with said channel region (alternatively, said second source region can well be defined as comprising the LDD region on its side, in which alternative rejection the contact is not merely electrical but also material).

3. ***Claims 42, 46, 49, 52, 55*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki et al and Yamazaki et al as applied to claims 41 and 45, respectively, above, and further in view of Patent Document owned by Sharp KK (Publication No.: JP 11101974 A). As detailed above, claims 41, 45, 48, 51, 54 are unpatentable over Miyazaki et al in view of Yamazaki et al. *Neither necessarily teach* the further limitation as defined by claims 42, 46, 49, 52, 55, respectively. *However, it would have been obvious* to include said further limitation in view of the Patent Document by Sharp KK, who teaches the application of liquid crystal display devices based on TFT transistors to (see Use): personal computers, portable information terminals, video apparatus, inter alia. Said application are thus seen to be obvious applications of the invention obtained by combining Miyazaki et al and Yamazaki et al.

Furthermore, claim 52 is a substantial duplicate of claim 46 (see "Double Patenting"), and hence the rejection of claim 46 must herewith be repeated verbatim for claim 52. Furthermore, claim 55 is a substantial duplicate of claim 49 (see "Double Patenting"), and hence the rejection of claim 46 must herewith be repeated verbatim for claim 55.

4. ***Claims 43, 47, 50, 53, 56*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki et al and Yamazaki et al as applied to claims 41, 45, 48, 51, 55, respectively, above, and further in view of Tang et al (5,684,365*). As detailed above, claims 41, 45 and 48 are unpatentable* over Miyazaki et al in view of Yamazaki et al. *Neither necessarily teach the further limitation* defined by claims 43, 47, 50, 53 and 56, respectively. *However, it would have been obvious* to include said further limitation in view of Tang et al, who, in a patent on a electroluminescence (EL) display teach the inclusion of TFT electroluminescent pixels for the specific purpose to eliminate the need to pattern the EL cathode, from which it follows that the invention by Miyazaki et al finds obvious applications to EL display devices. *Motivation* thus stems from the immediate and obvious applicability of the invention by Miyazaki et al to the field of EL display technology. Furthermore, claim 53 is a substantial duplicate of claim 47 (see "Double Patenting"), and hence the rejection of claim 47 must herewith be repeated verbatim for claim 52. Also, claim 56 is a substantial duplicate of claim 50 (see "Double Patenting"), and hence the rejection of claim 50 must herewith be repeated verbatim for claim 56.

5. ***Claim 62-66*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki et al and Yamazaki et al as applied to claim 41 above, and further in view of Yamazaki et al (5,784,073), henceforth referred to as Yamazaki2. *As detailed above, claims 41, 45, 48, 51 and 54 are unpatentable over Miyazaki et al in view of Yamazaki et al.*

Furthermore, Miyazaki et al teach that said semiconductor device further comprises:

a first insulating film 207 (cf. Figure 7 and col. 9, l. 16-30) over said first, second, and third gate electrodes;

a second insulating film 217 (cf. Figure 7 and col. 10, l. 30-35) over said first insulating film;

and

a pixel electrode 13, 508 (cf. Figures 1 and 7) (cf. col. 8, l. 7-25 and col. 10, l. 63 – col. 11, l. 1) over said second insulating film connected to said first semiconductor layer (i./e, the layer of the pixel TFT: this is what makes said TFT3 a pixel TFT, being inherent in the pixel TFT3).

Neither Miyazaki et al nor Yamazaki et al necessarily teach the further limitation as defined by claims 62-66, namely: of a third insulation film comprising organic resin over said second insulating film, with said pixel electrode also being over said third insulating film.

However, it would have been obvious to include said further limitation in view of *Yamazaki2*, who, in a patent on an electro-optical device based on thin film transistors

(col. 3, l. 33 – col. 4, l. 25), - hence closely related to the invention by Miyazaki et al, teach the inclusion of an organic resin layer 119 for the specific purpose of flattening prior to forming the pixel electrode thereon (cf. col. 16, l. 16-35).

Motivation, to include the teaching by Yamazaki2 in the invention by Miyazaki et al, lies in the resulting substantially flat surface over which the pixel electrode can be laid, thus reducing the abrasiveness, and with it the mechanical vulnerability, of the structure. Furthermore, the mechanical contact between the pixel electrode and the insulating material is enhanced through the planarization, thus increasing mechanical integrity.

Double Patenting

6. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

7. Applicant is advised that should claim 45 be found allowable, claim 51 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing

one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

8. Applicant is advised that should claim 46 be found allowable, claim 52 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

9. Applicant is advised that should claim 47 be found allowable, claim 53 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

10. Applicant is advised that should claim 48 be found allowable, claim 54 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

11. Applicant is advised that should claim 49 be found allowable, claim 55 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two

claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

12. Applicant is advised that should claim 50 be found allowable, claim 56 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
December 30, 2004

Patent Examiner:

Johannes Mondt (Art Unit: 2826)